Amendment to Specification

Please amend the Abstract on page 23 as follows:

A method and apparatus for real-time derivation of precise digital clock edges and synchronous logic samples ~~from multi-bit analog samples~~ from a digital signal having a clock channel and at least one data channel acquires a plurality of temporally offset analog samples during each of a sequence of sample periods and from consecutive samples where there is a logic level transition estimates an edge time. From the edge times for the clock channel an offset is added and applied to the at least one data channel to determine the synchronous logic samples for the data channel at each offset clock edge time.